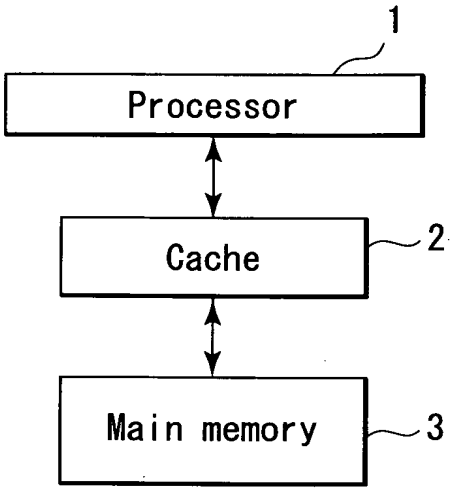


FIG. 1A (PRIOR ART)

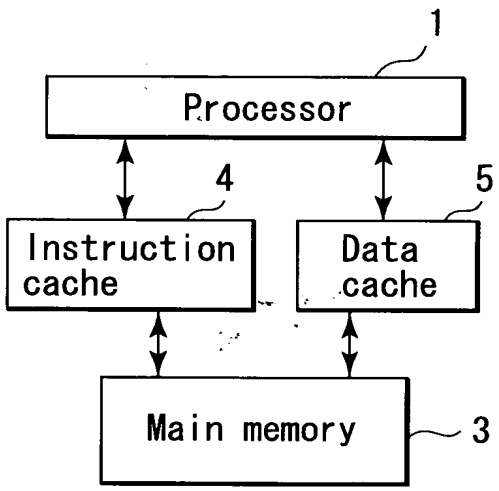


FIG. 1B (PRIOR ART)

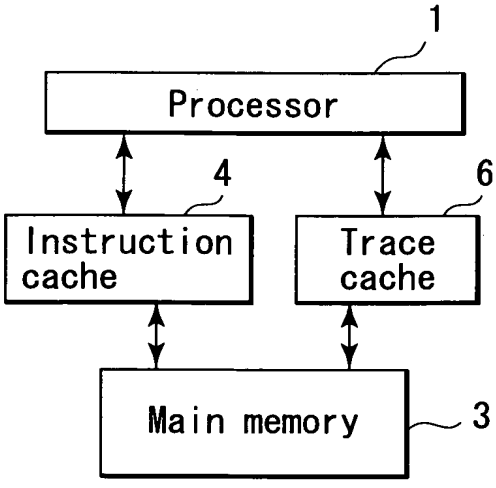


FIG. 1C (PRIOR ART)

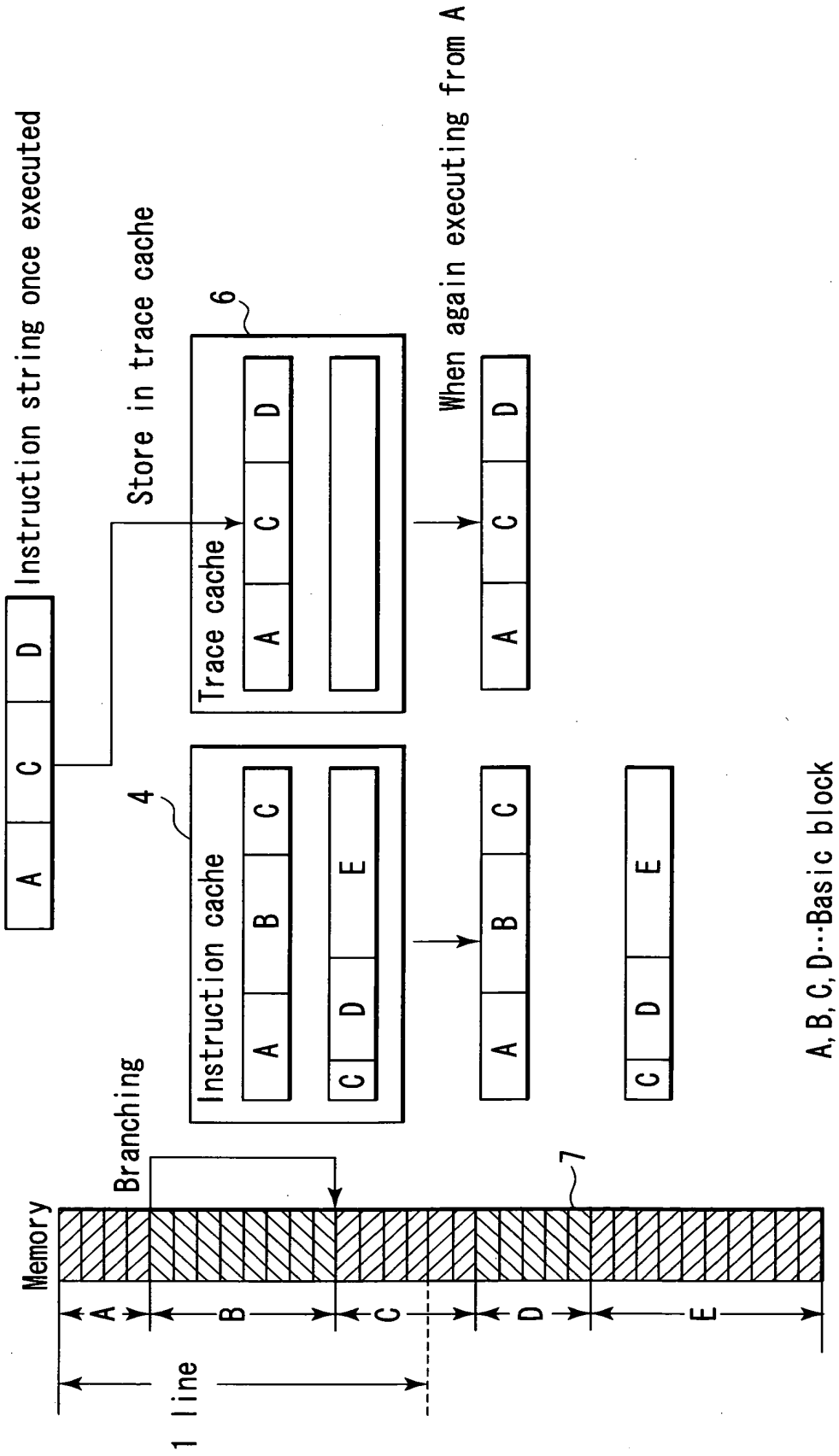


FIG. 2 (PRIOR ART)

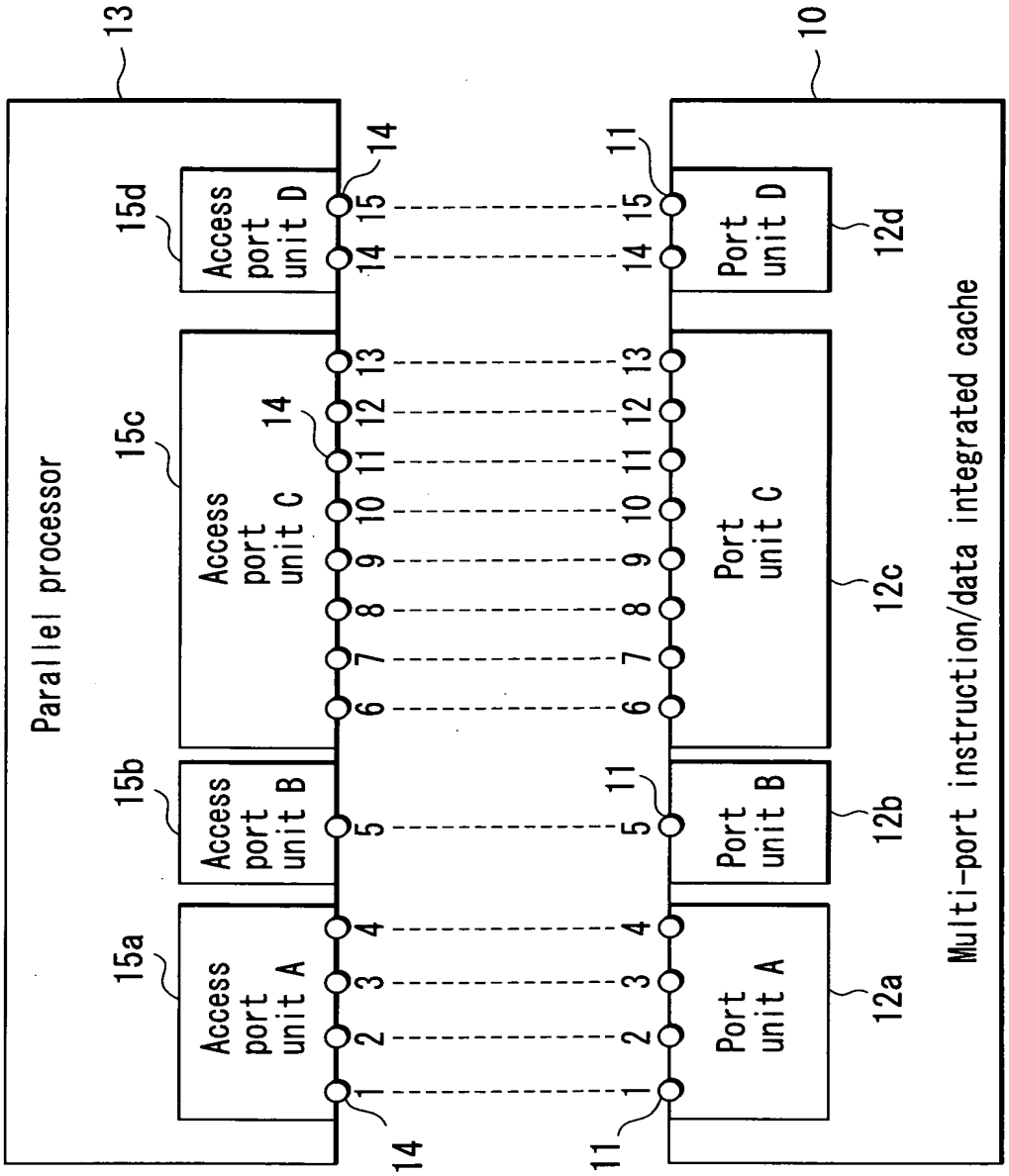
13
Parallel processor
15a
Access port unit A
15b
Access port unit B
15c
Access port unit C
15d
Access port unit D
14
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
10
Multi-port instruction/data integrated cache
12a
Port unit A
12b
Port unit B
12c
Port unit C
12d
Port unit D
11
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

FIG. 3

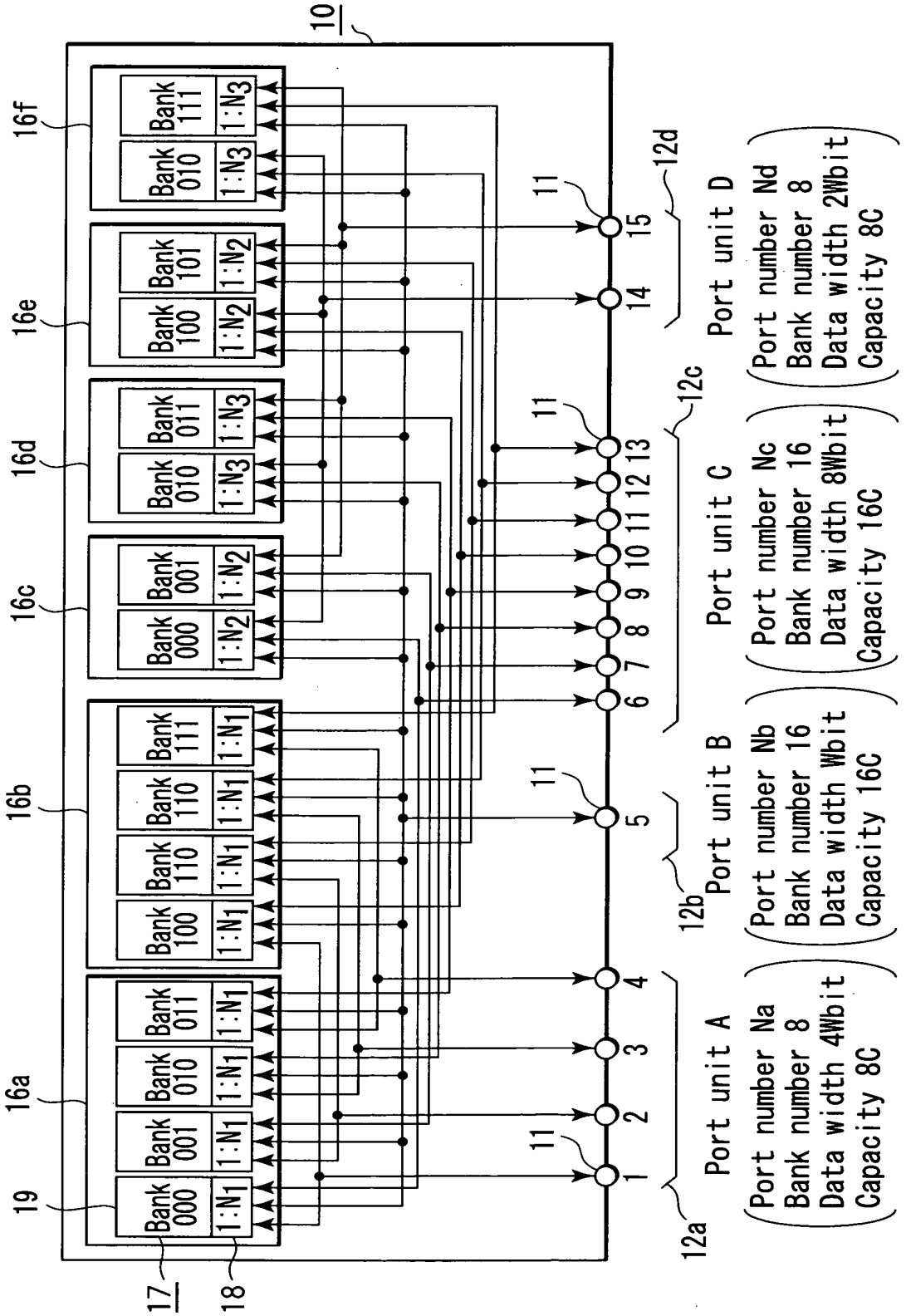
10
16a
16b
16c
16d
16e
16f
17
18
19
Bank 000
Bank 001
Bank 010
Bank 011
Bank 100
Bank 110
Bank 111
Bank 000
Bank 001
Bank 010
Bank 011
Bank 100
Bank 101
Bank 110
Bank 111
1:N1
1:N2
1:N3
11
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
12a
12b
12c
12d
Port unit A
Port number Na
Bank number 8
Data width 4Wbit
Capacity 8C
Port unit B
Port number Nb
Bank number 16
Data width Wbit
Capacity 16C
Port unit C
Port number Nc
Bank number 16
Data width 8Wbit
Capacity 16C
Port unit D
Port number Nd
Bank number 8
Data width 2Wbit
Capacity 8C
* Data width Wbit of each bank, bank capacity C, N1=Na+Nb+Nc, N2=Nb+Nc+Nd

FIG. 4

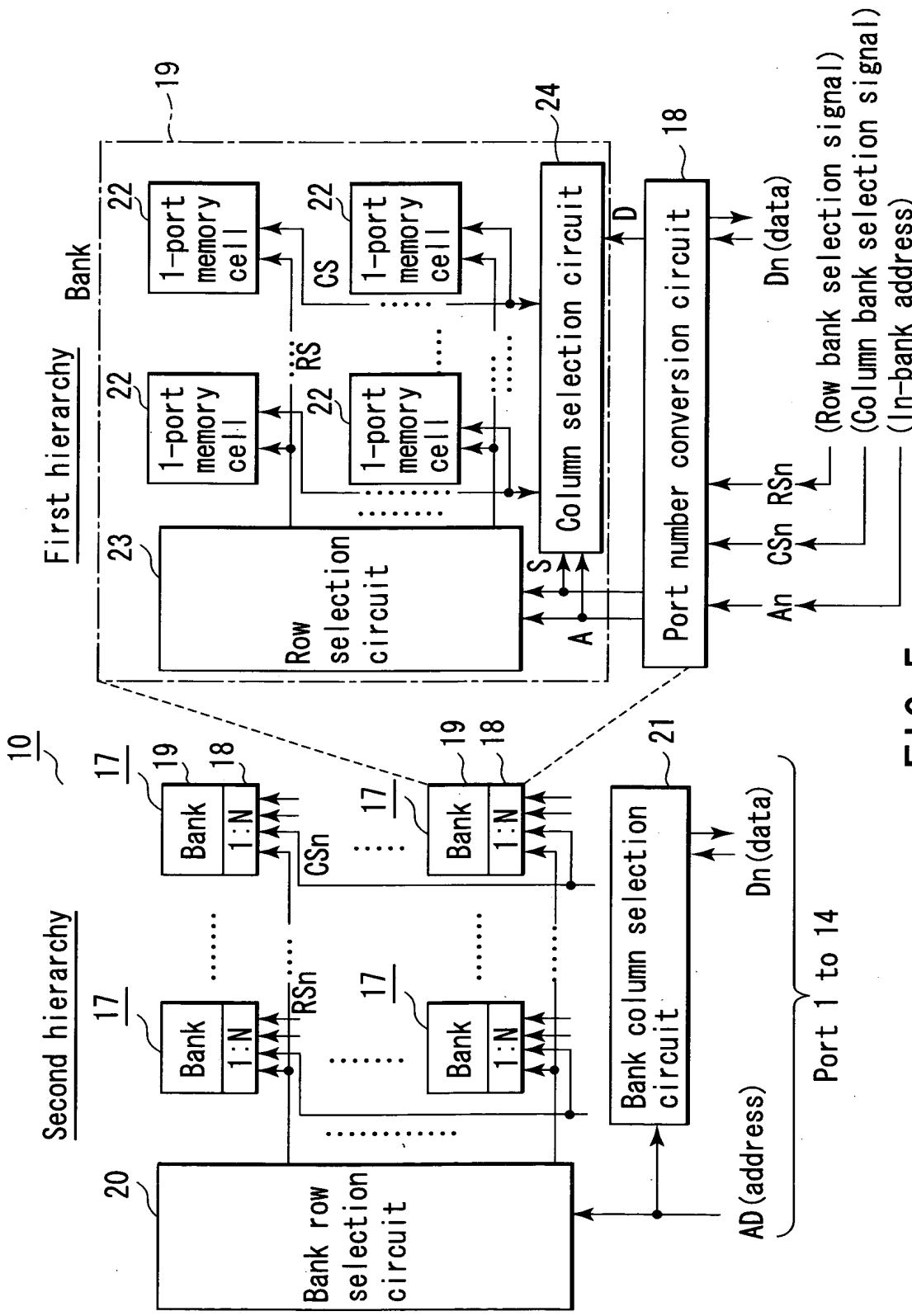
10
First hierarchy
Second hierarchy
Bank
19
22
1-port memory cell
CS
RS
23
Row selection circuit
24
Column selection circuit
18
Port number conversion circuit
D
S
A
Dn(data)
(Row bank selection signal)
(Column bank selection signal)
(In-bank address)
An
CSn
RSn
17
1:N
CSn
RSn
20
Bank row selection circuit
21
Bank column selection circuit
AD(address)
Port 1 to 14

FIG. 5

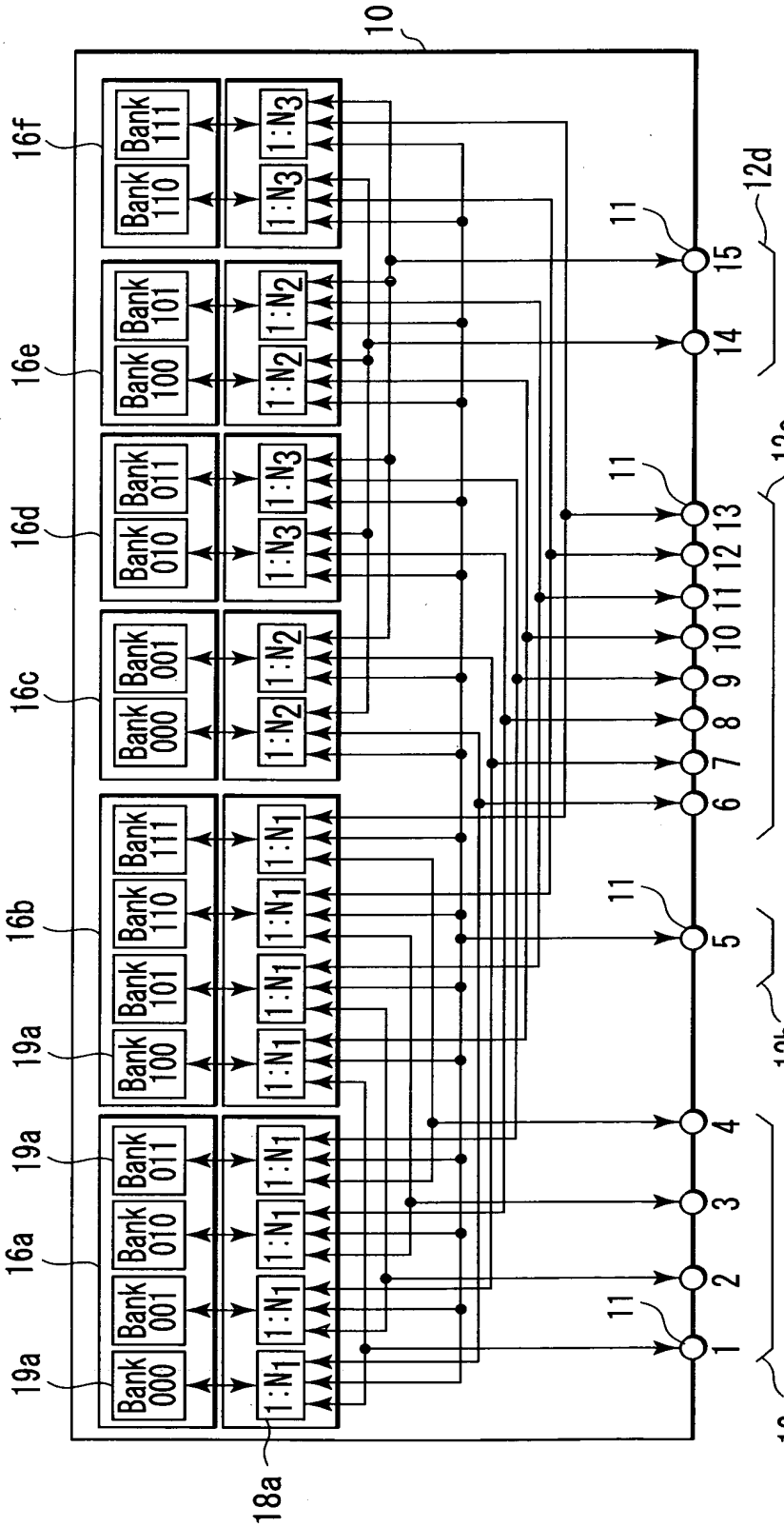
10
16f
16e
16d
16c
16b
16a
19a
18a
Bank 000
Bank 001
Bank 010
Bank 011
Bank 100
Bank 101
Bank 110
Bank 111
1:N1
1:N2
1:N3
11
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
12a
12b
12c
12d
Port unit A
Port number Na
Bank number 8
Data width 4Wbit
Capacity 8C
Port unit B
Port number Nb
Bank number 16
Data width Wbit
Capacity 16C
Port unit C
Port number Nc
Bank number 16
Data width 8Wbit
Capacity 16C
Port unit D
Port number Nd
Bank number 8
Data width 2Wbit
Capacity 8C
* Data width Wbit of each bank, bank capacity C, N1=Na+Nb+Nc, N2=Nb+Nc+Nd

FIG. 6

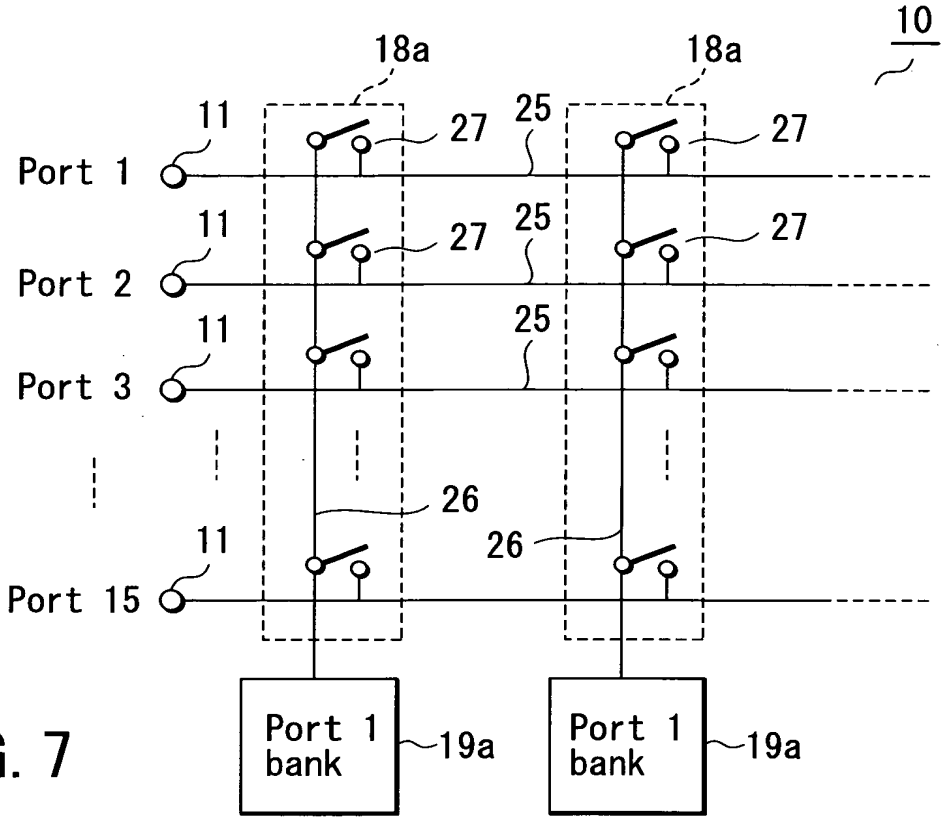
10
18a
18a
11
27
25
27
Port 1
11
27
25
27
Port 2
11
25
Port 3
26
26
11
Port 15
Port 1 bank
19a
Port 1 bank
19a

FIG. 7

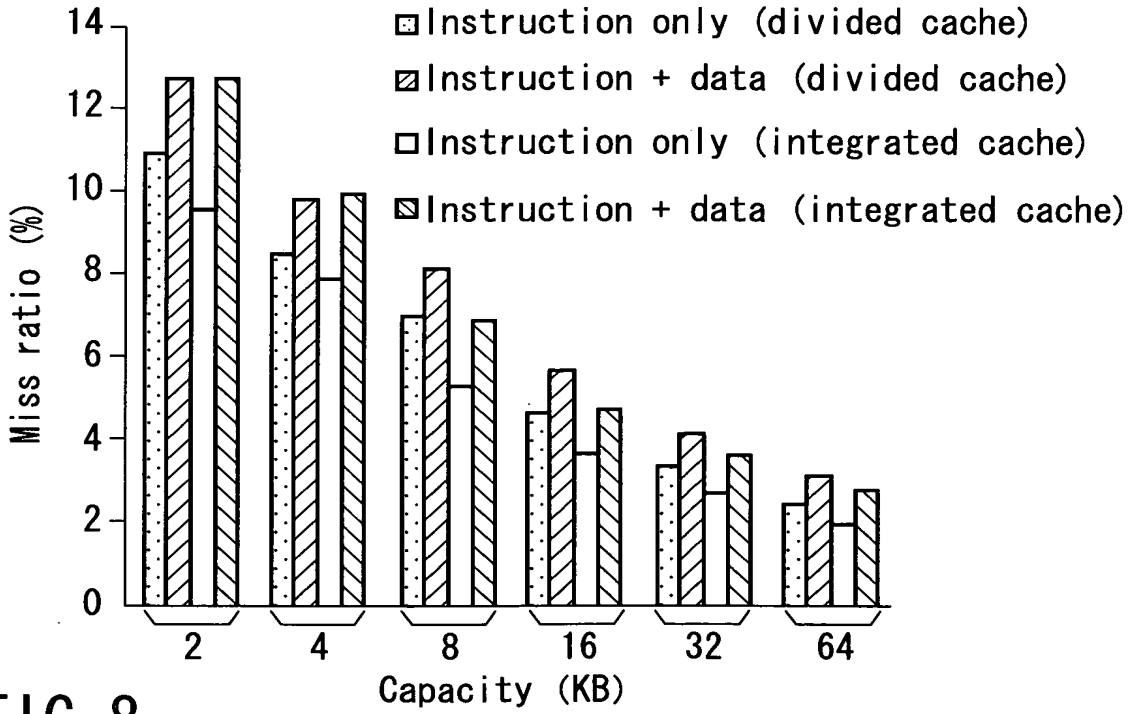
Instruction only (divided cache)
Instruction + data (divided cache)
Instruction only (integrated cache)
Instruction + data (integrated cache)
Miss ratio (%)
0
2
4
6
8
10
12
14
2
4
8
16
32
64
Capacity (KB)

FIG. 8

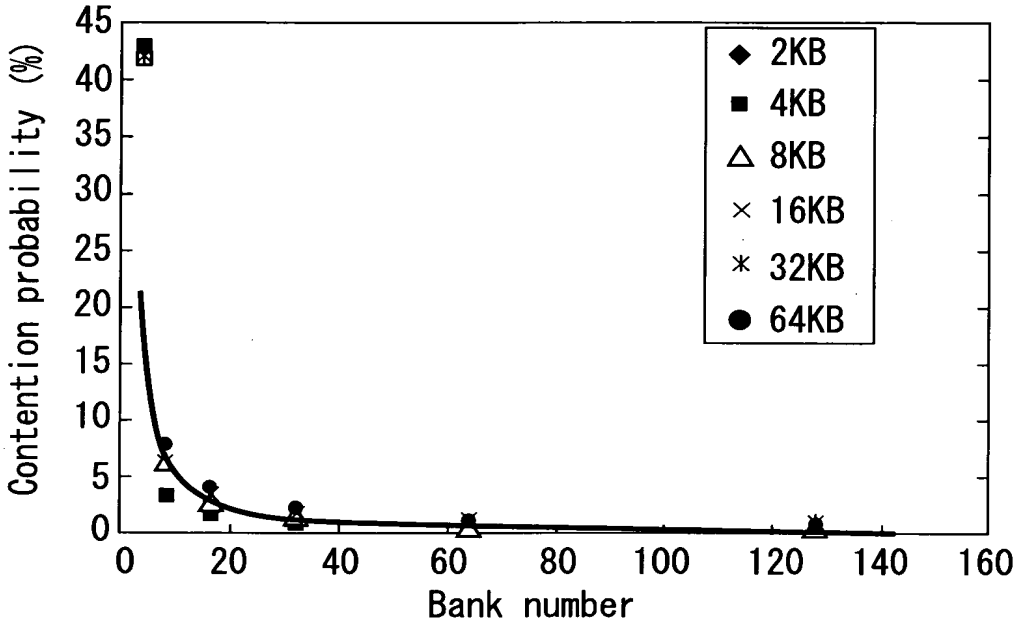
Contention probability (%)
45
40
35
30
25
20
15
10
5
0
0
20
40
60
80
100
120
140
160
Bank number
2KB
4KB
8KB
16KB
32KB
64KB

FIG. 9

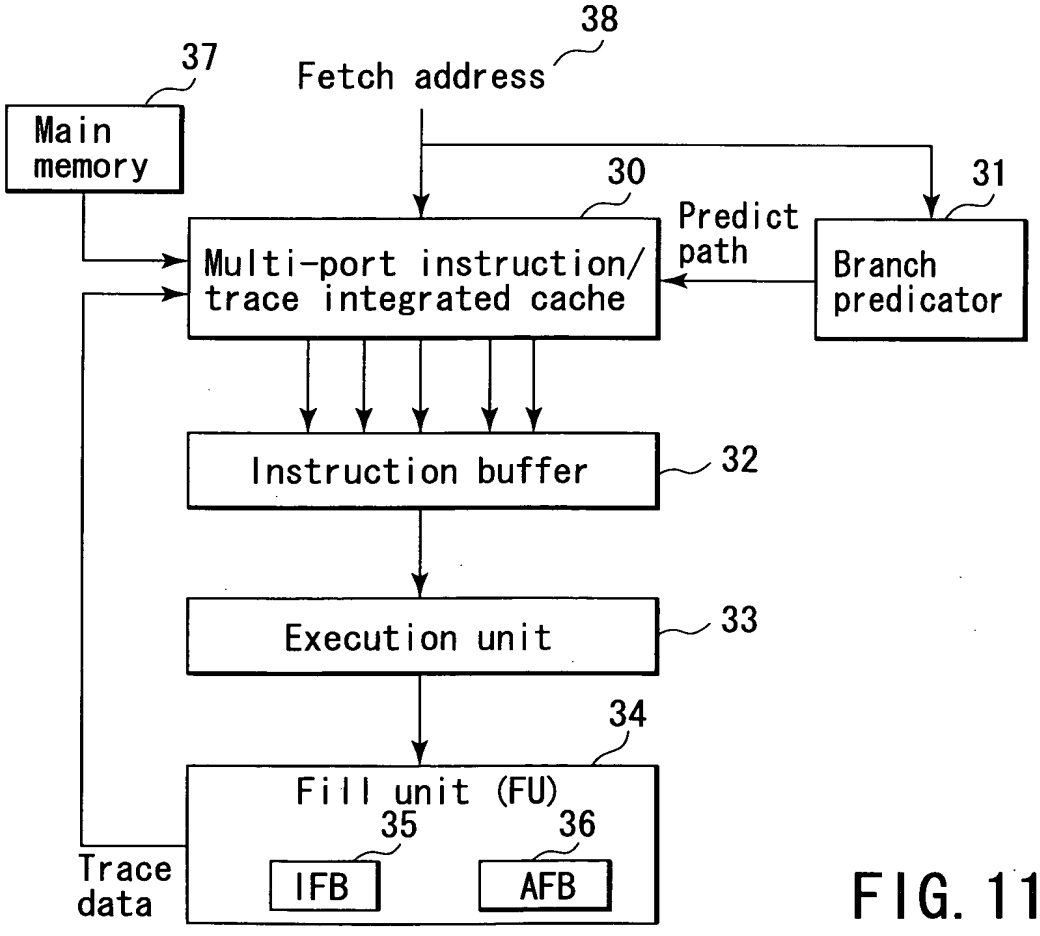
38
Fetch address
37
Main memory
30
31
Predict path
Multi-port instruction/ trace integrated cache
Branch predicator
Instruction buffer
32
Execution unit
33
34
Fill unit (FU)
35
36
IFB
AFB
Trace data

FIG. 11

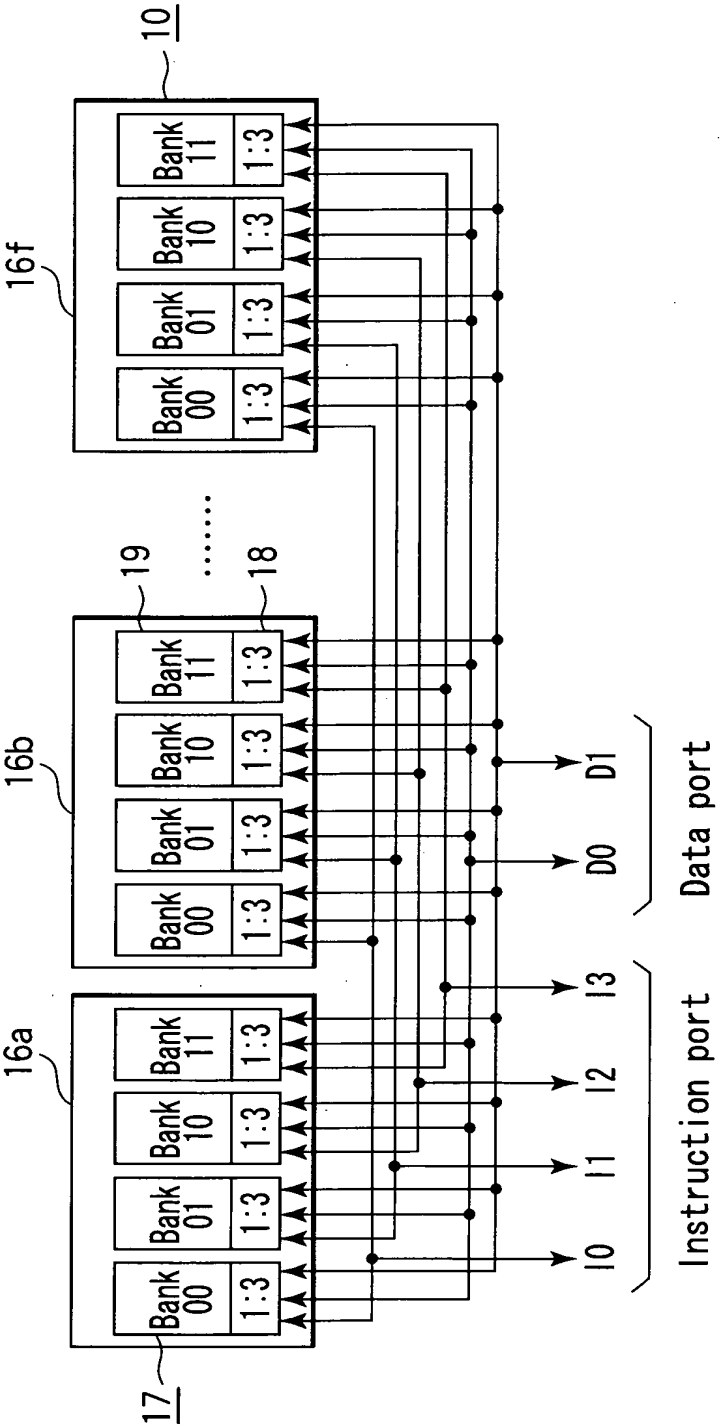
10
16f
16b
16a
17
19
18
Bank 00
Bank 01
Bank 10
Bank 11
1:3
I0
I1
I2
I3
D0
D1
Instruction port
Data port

FIG. 10

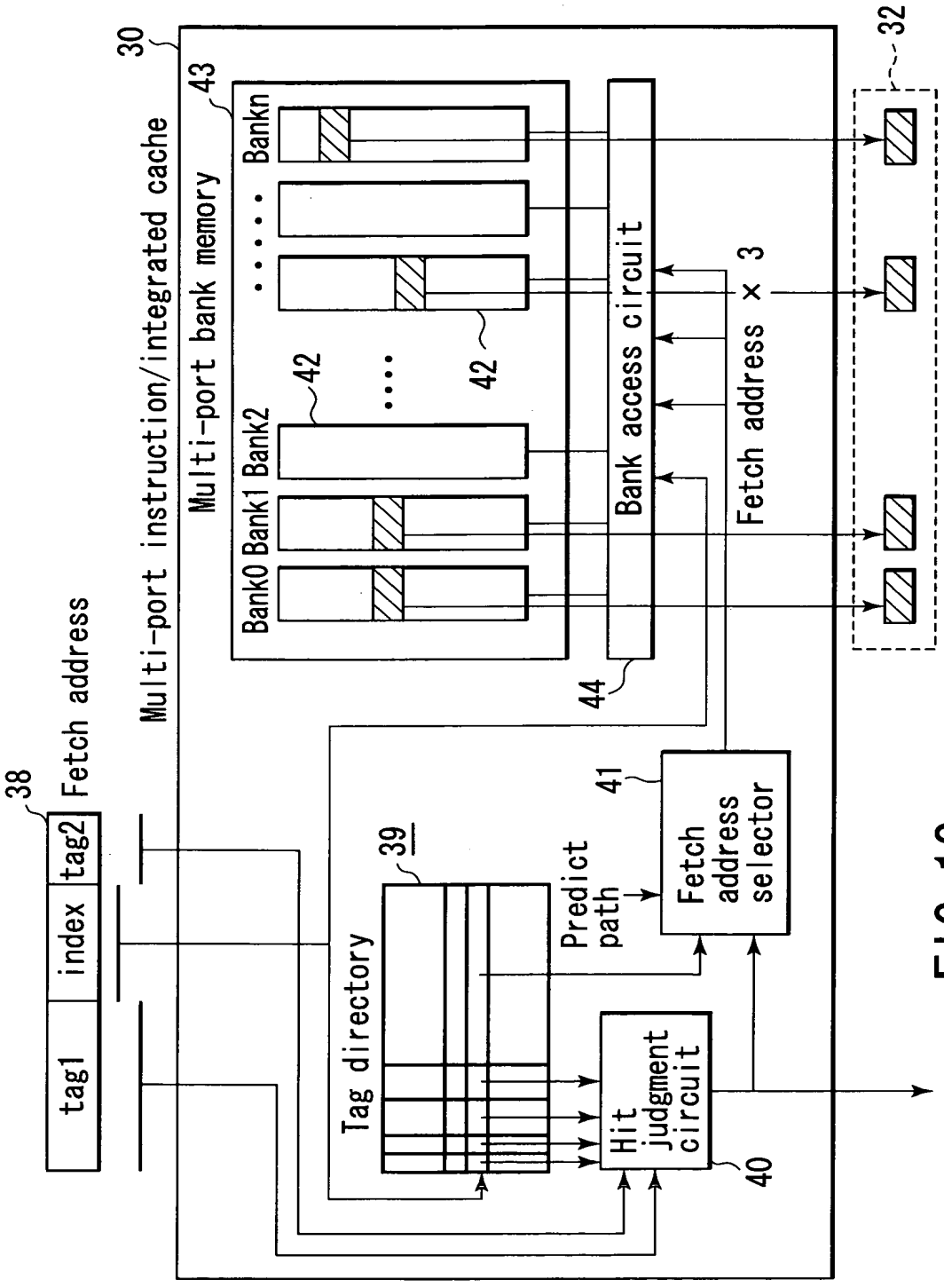
30
Multi-port instruction/integrated cache
43
Multi-port bank memory
Bank0
Bank1
Bank2
Bankn
42
42
Bank access circuit
44
32
Fetch address × 3
38
Fetch address
tag1
index
tag2
39
Tag directory
Predict path
41
Fetch address selector
Hit judgment circuit
40

FIG. 12

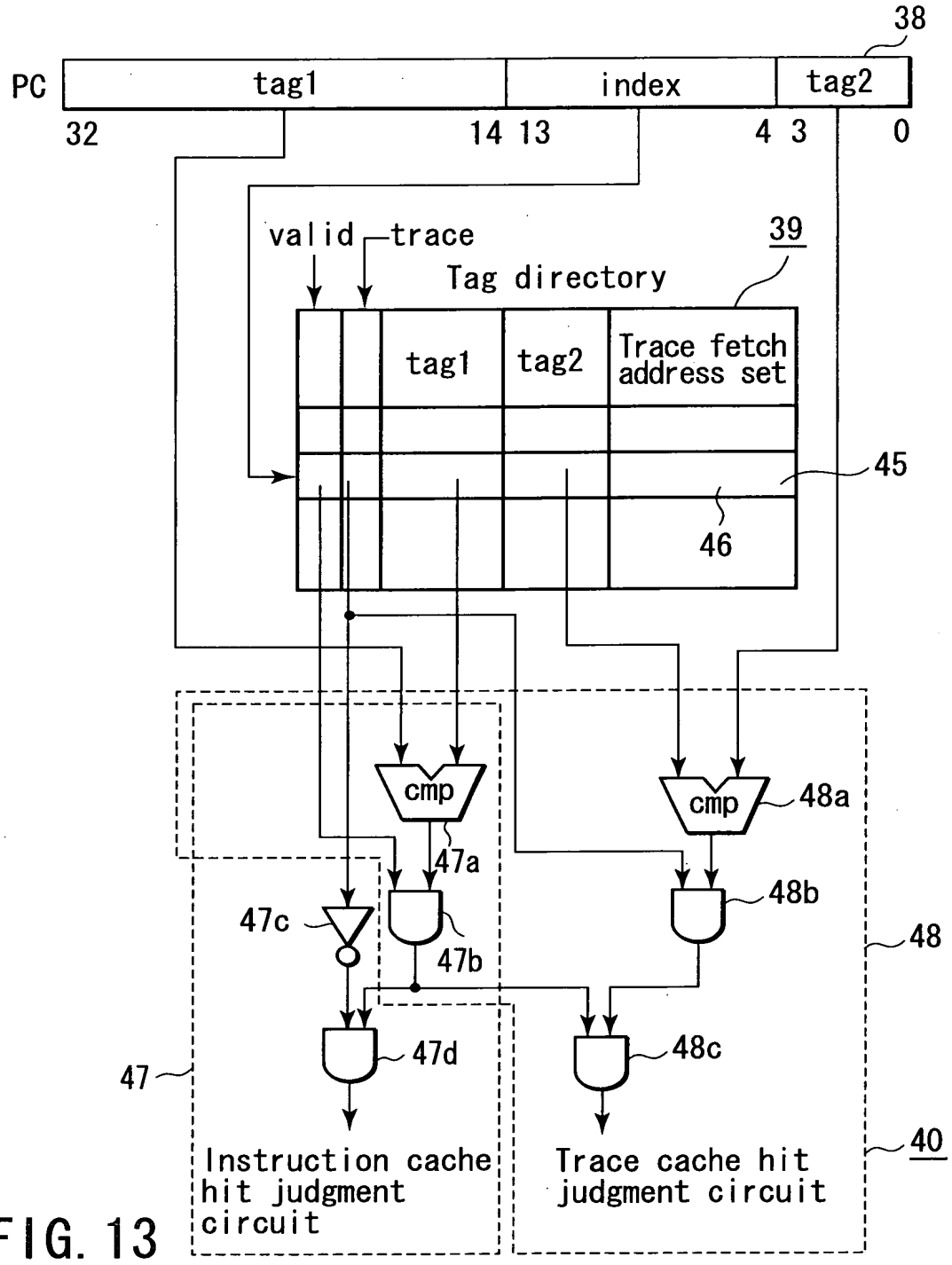
38
PC
tag1
index
tag2
32
14 13
4 3
0
valid
trace
39
Tag directory
tag1
tag2
Trace fetch address set
45
46
cmp
cmp
48a
47a
48b
47c
47b
48
47d
48c
47
Instruction cache hit judgment circuit
Trace cache hit judgment circuit
40

FIG. 13

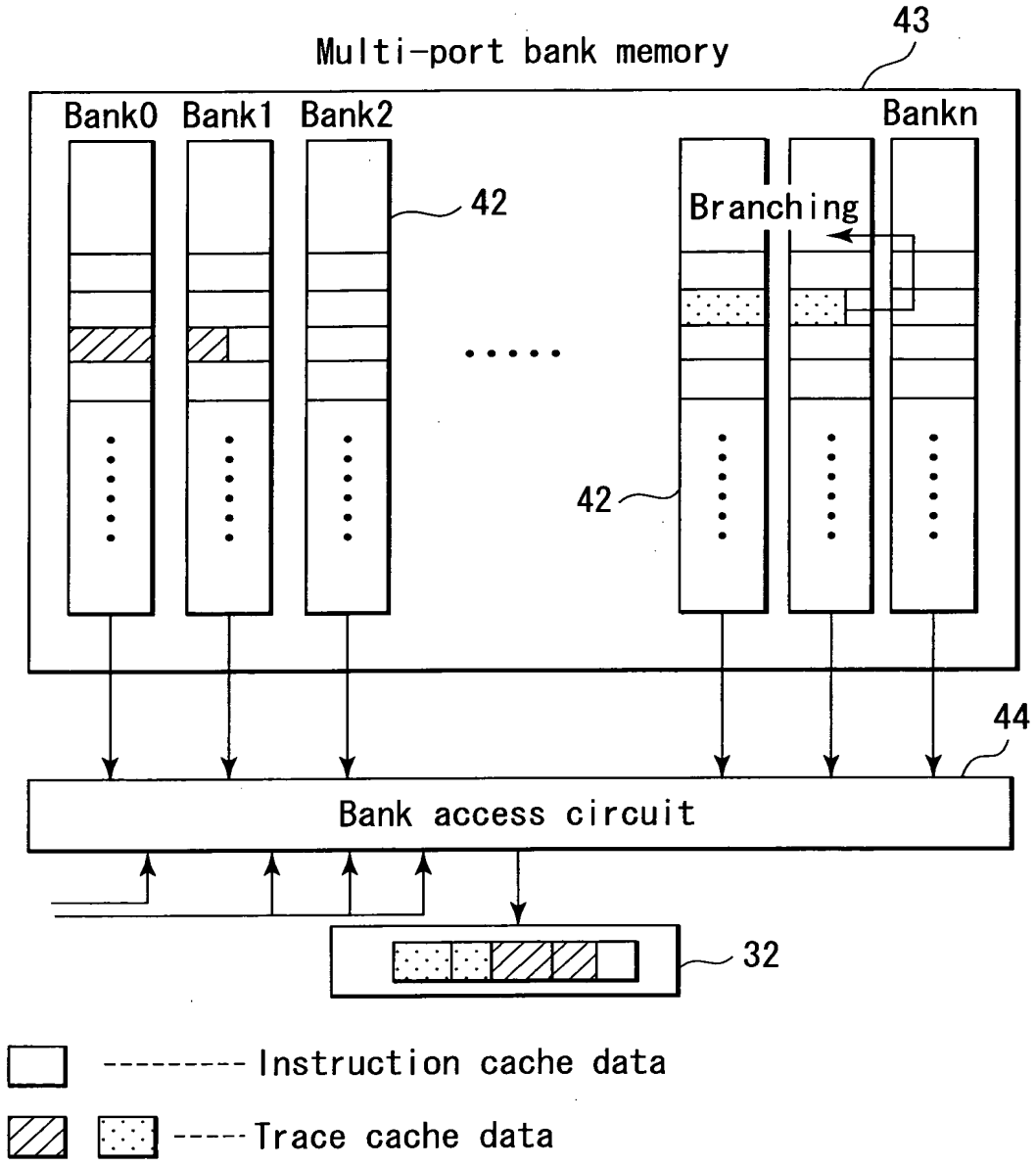
Multi-port bank memory
43
Bank0
Bank1
Bank2
Bankn
42
Branching
42
44
Bank access circuit
32
Instruction cache data
Trace cache data

FIG. 14

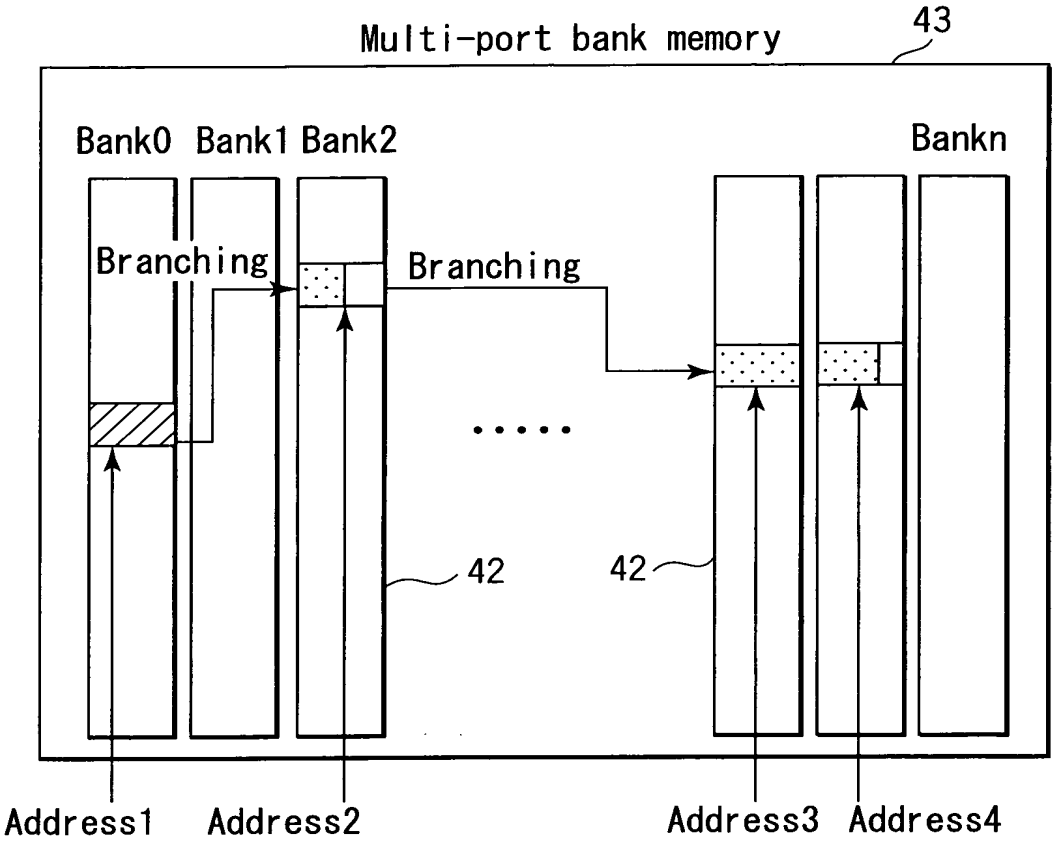
Multi-port bank memory
43
Bank0
Bank1
Bank2
Bankn
Branching
Branching
42
42
Address1
Address2
Address3
Address4

FIG. 15

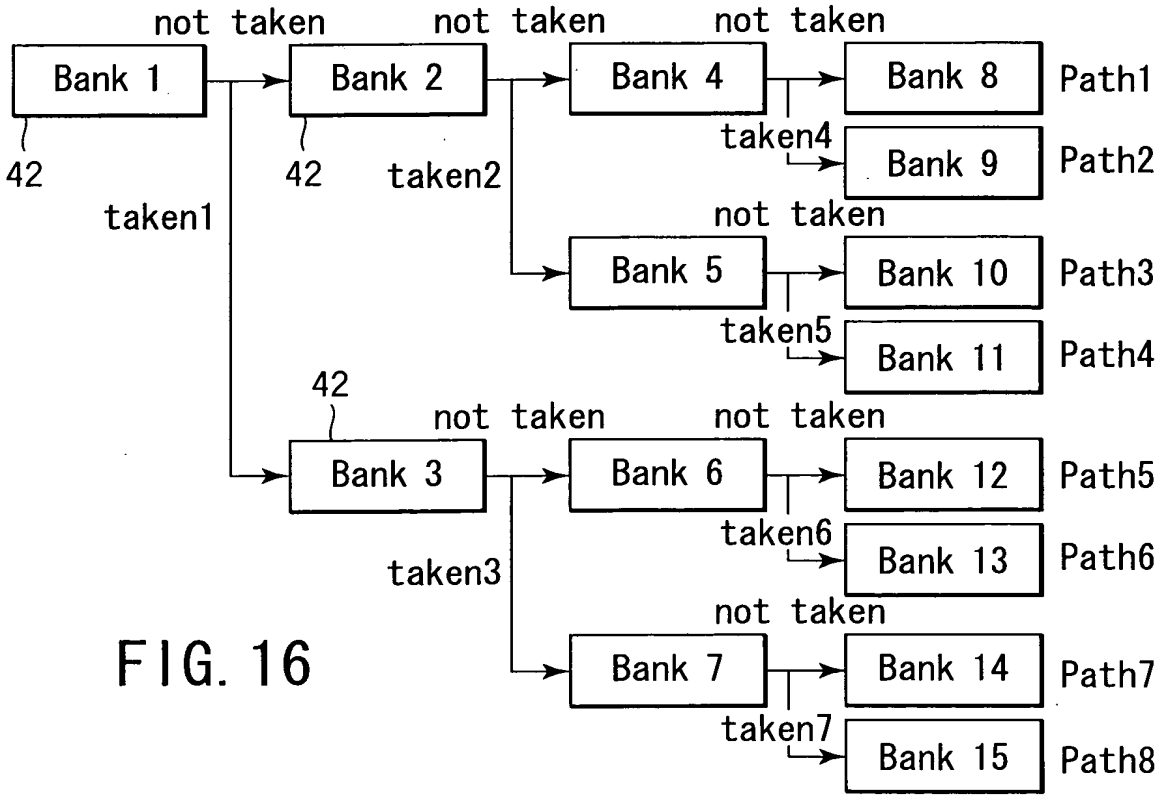
not taken
not taken
not taken
Bank 1
Bank 2
Bank 4
Bank 8
Path1
taken4
Bank 9
Path2
42
42
taken2
taken1
not taken
Bank 5
Bank 10
Path3
taken5
Bank 11
Path4
42
not taken
not taken
Bank 3
Bank 6
Bank 12
Path5
taken6
Bank 13
Path6
taken3
not taken
Bank 7
Bank 14
Path7
taken7
Bank 15
Path8

FIG. 16

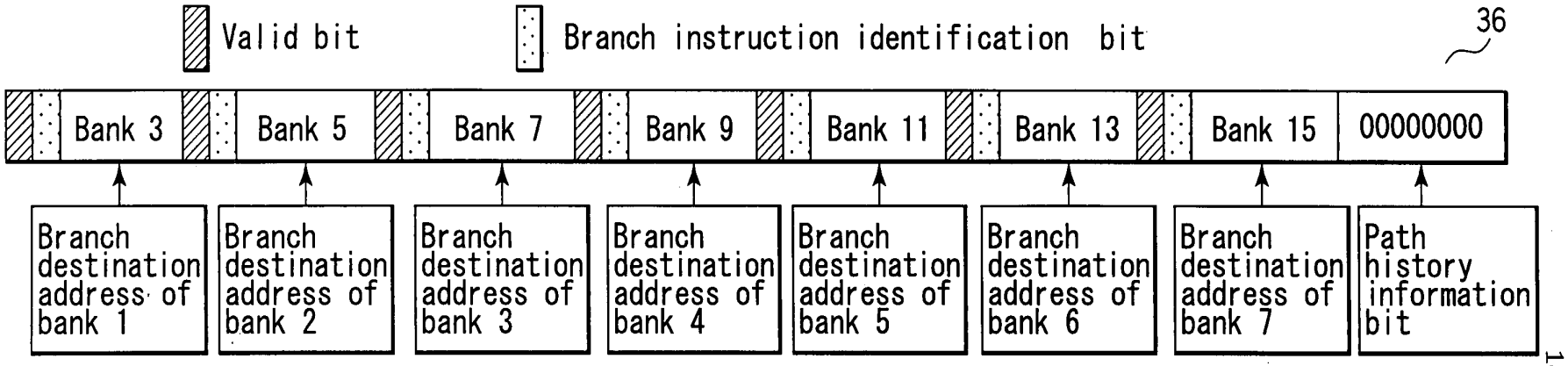


FIG. 17

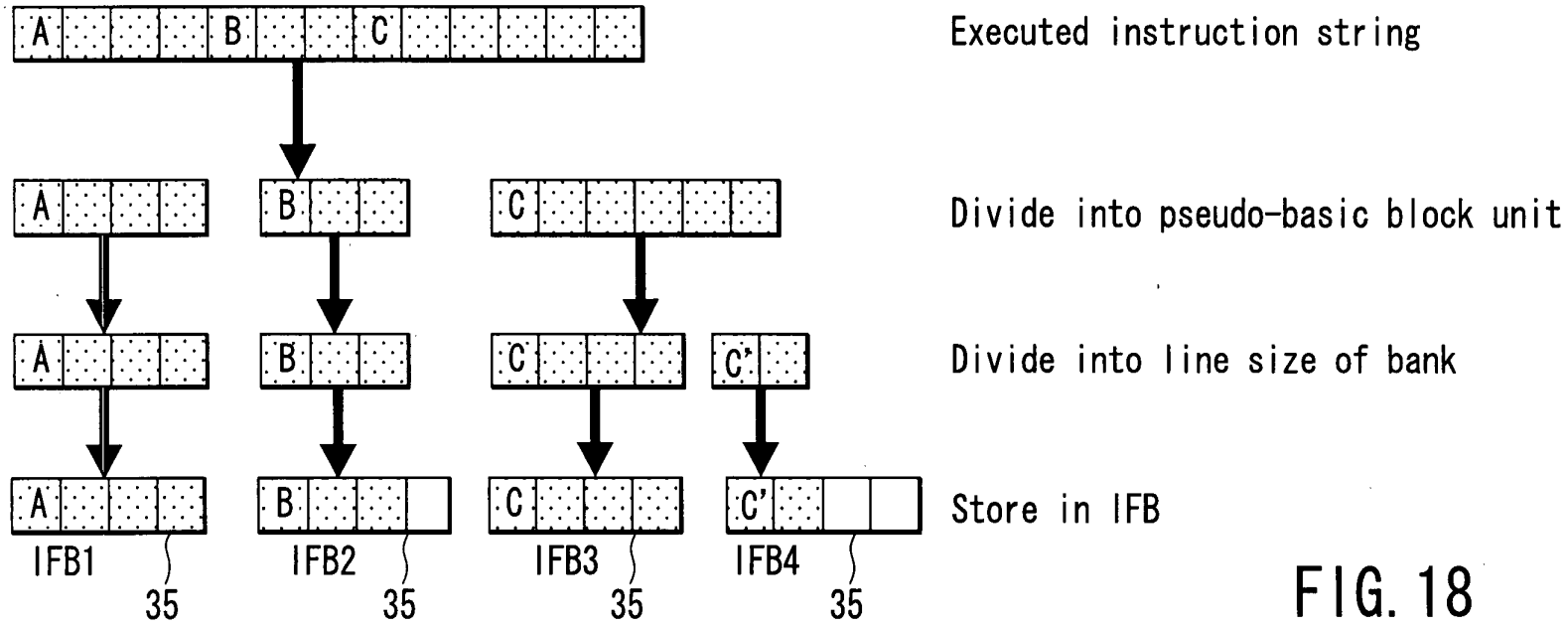


FIG. 18



Title: MULTI-PORT INTEGRATED CACHE
Inventors: T. Hironaka et al.
Docket No.: SUSU121842

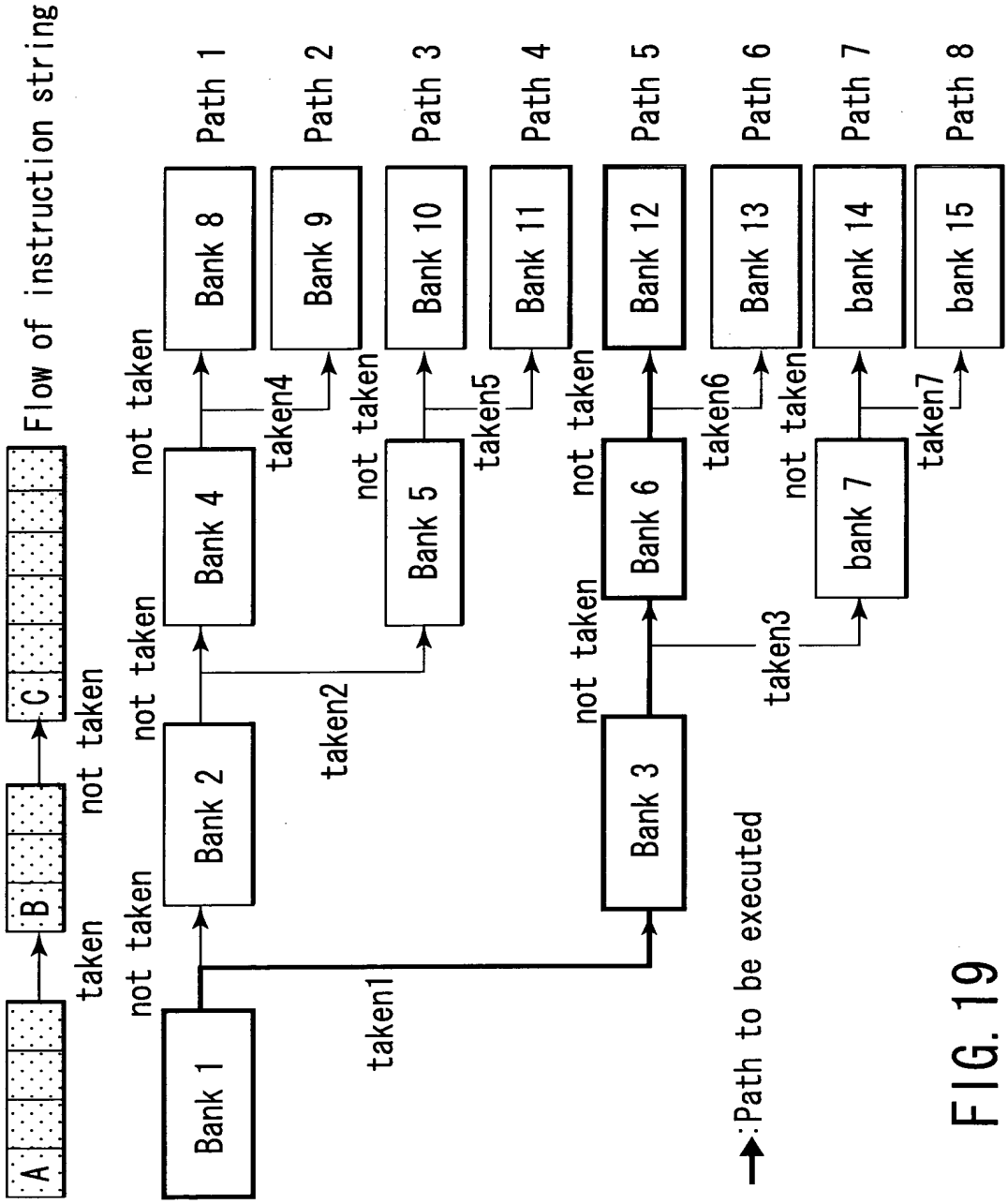
Flow of instruction string
A
B
C
taken
not taken
Bank 1
Bank 2
Bank 3
Bank 4
Bank 5
Bank 6
Bank 7
Bank 8
Bank 9
Bank 10
Bank 11
Bank 12
Bank 13
bank 14
bank 15
taken1
taken2
taken3
taken4
taken5
taken6
taken7
Path 1
Path 2
Path 3
Path 4
Path 5
Path 6
Path 7
Path 8
:Path to be executed

FIG. 19

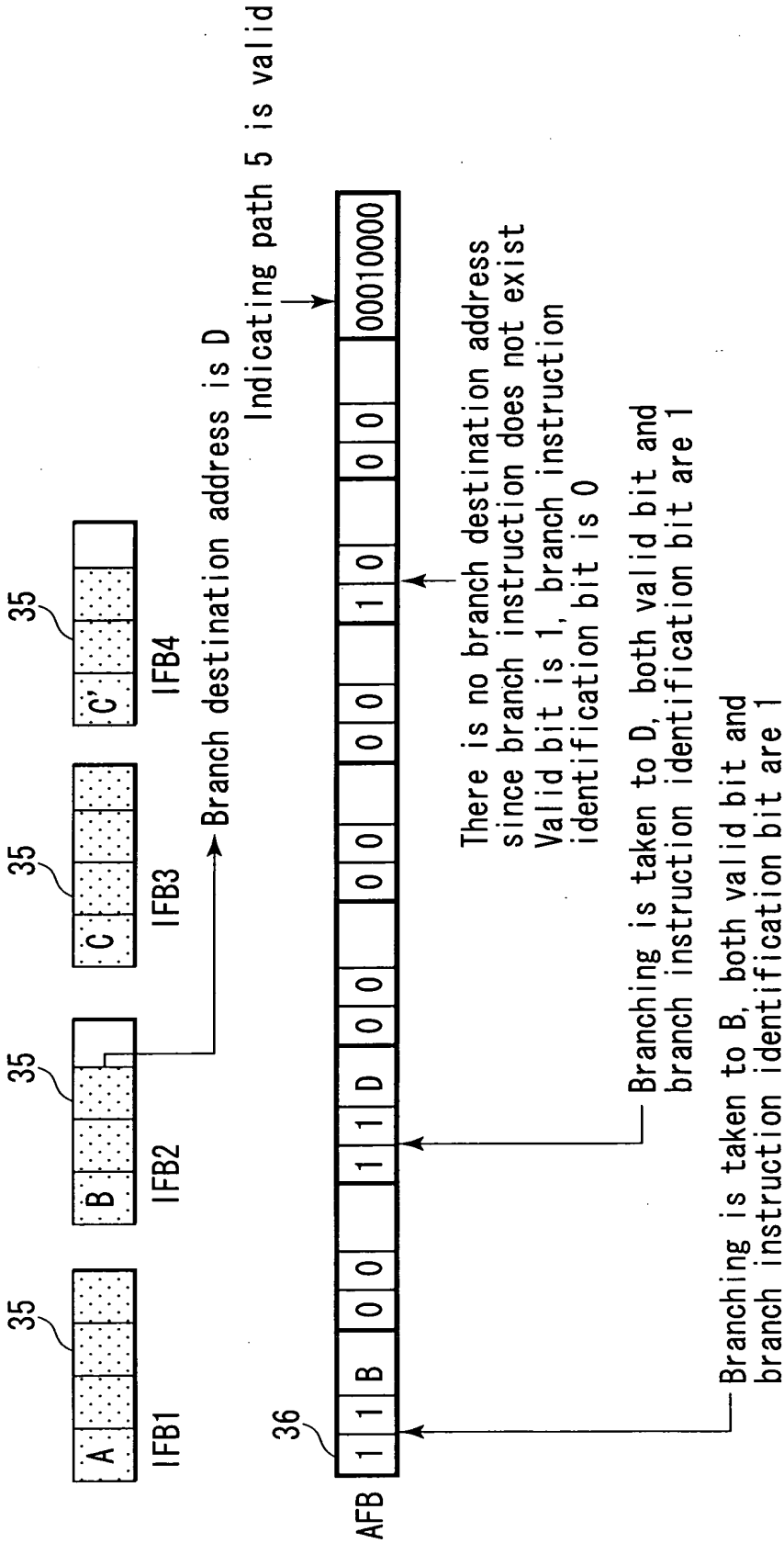
Indicating path 5 is valid
Branch destination address is D
There is no branch destination address since branch instruction does not exist
Valid bit is 1, branch instruction identification bit is 0
Branching is taken to D, both valid bit and branch instruction identification bit are 1
Branching is taken to B, both valid bit and branch instruction identification bit are 1
AFB
IFB1
IFB2
IFB3
IFB4
35
36
A
B
C
C'
1 1 B 0 0
1 1 D 0 0
0 0
1 0
0 0
0 0
00010000

FIG. 20

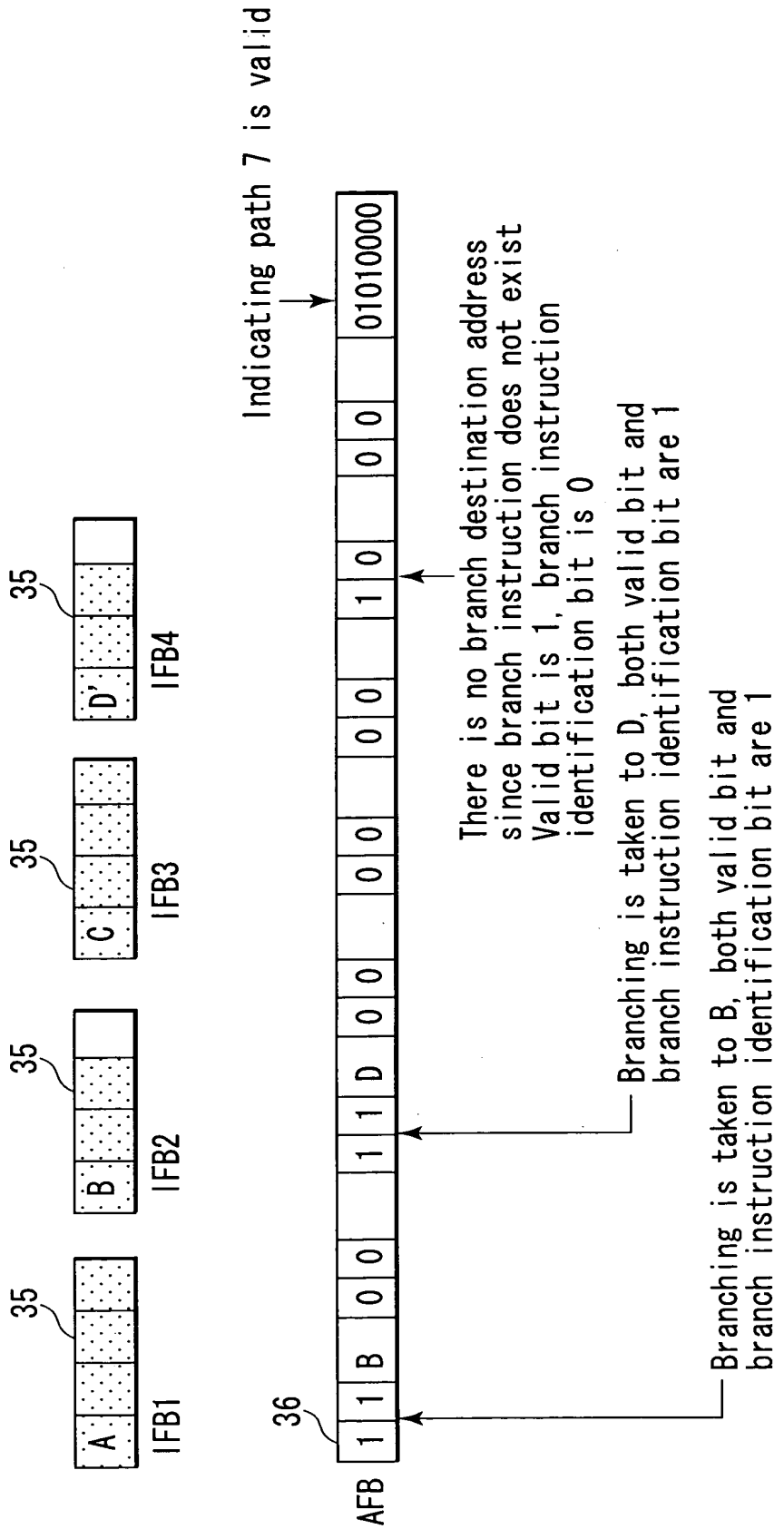
Indicating path 7 is valid
35
35
35
35
A
B
C
D'
IFB1
IFB2
IFB3
IFB4
36
1 1 B 0 0 1 1 D 0 0 0 0 0 1 0 0 0 01010000
AFB
There is no branch destination address since branch instruction does not exist
Valid bit is 1, branch instruction identification bit is 0
Branching is taken to D, both valid bit and branch instruction identification bit are 1
Branching is taken to B, both valid bit and branch instruction identification bit are 1

FIG. 21

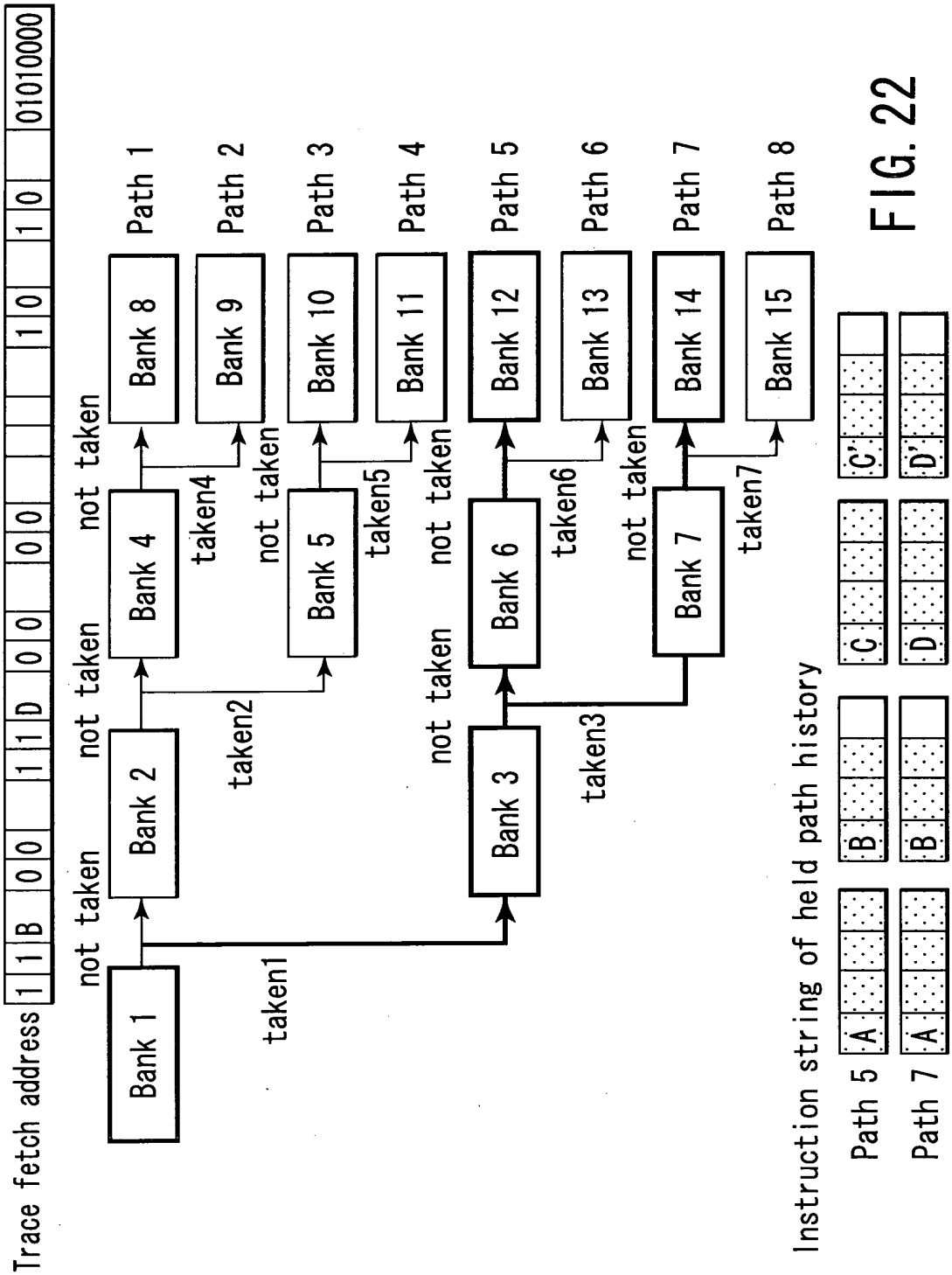
Trace fetch address
1 1 B 0 0 1 1 D 0 0 0 0 1 0 1 0 01010000
Bank 1
Bank 2
Bank 3
Bank 4
Bank 5
Bank 6
Bank 7
Bank 8
Bank 9
Bank 10
Bank 11
Bank 12
Bank 13
Bank 14
Bank 15
not taken
taken1
not taken
taken2
not taken
taken3
not taken
taken4
not taken
taken5
not taken
taken6
not taken
taken7
Path 1
Path 2
Path 3
Path 4
Path 5
Path 6
Path 7
Path 8
Instruction string of held path history
Path 5
A
B
C
C'
Path 7
A
B
D
D'

FIG. 22

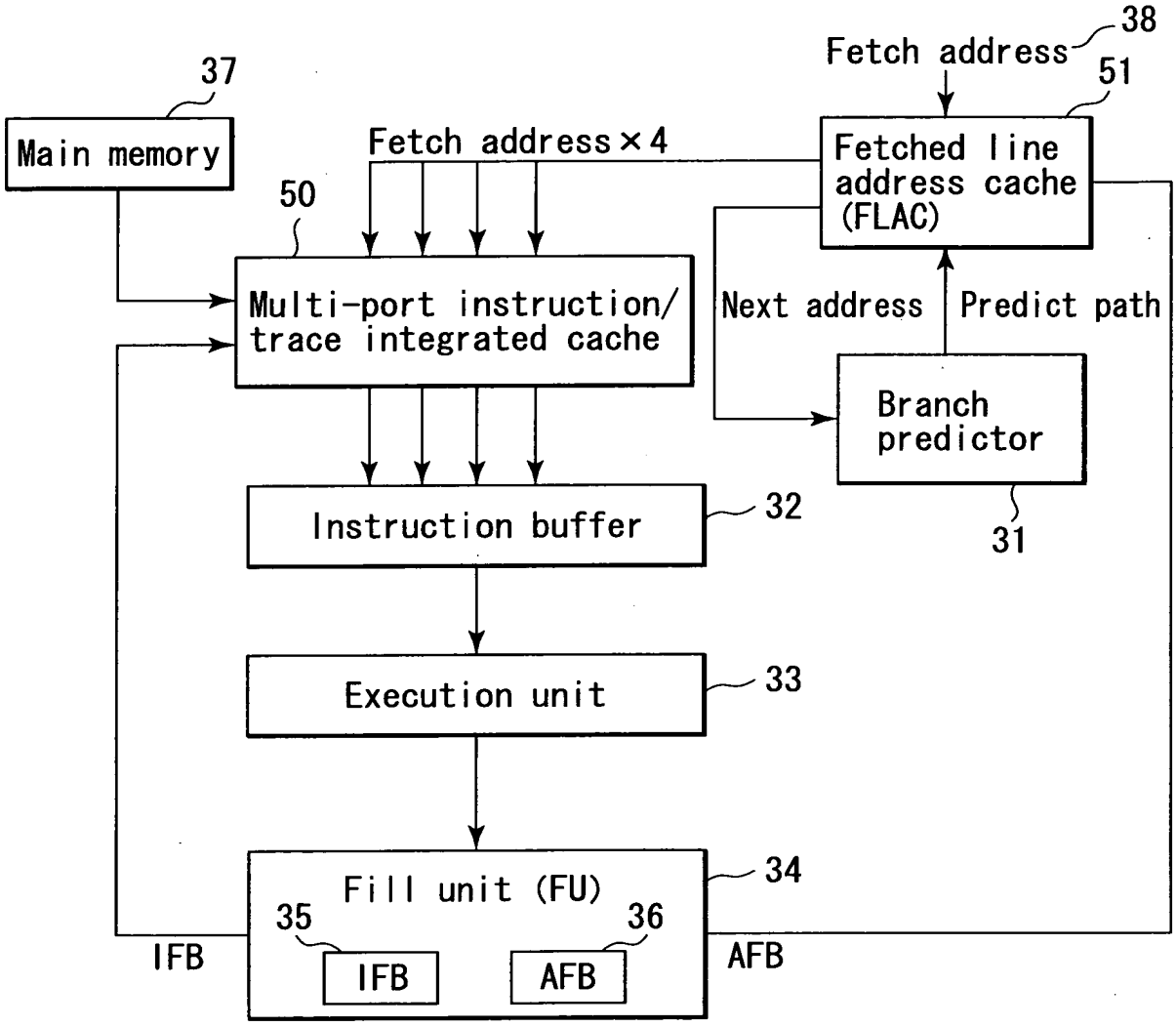
Main memory
37
Fetch address
38
51
Fetch address × 4
Fetched line address cache (FLAC)
50
Multi-port instruction/ trace integrated cache
Next address
Predict path
Branch predictor
31
Instruction buffer
32
Execution unit
33
Fill unit (FU)
34
35
36
IFB
AFB
IFB
AFB

FIG. 23

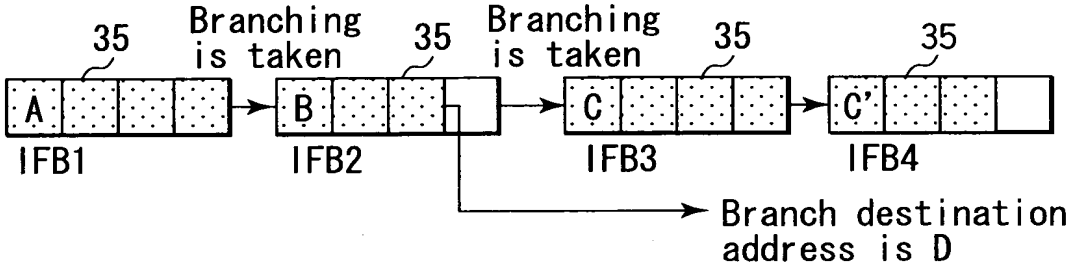
35
Branching is taken
35
Branching is taken
35
35
A
B
C
C'
IFB1
IFB2
IFB3
IFB4
Branch destination address is D

FIG. 24

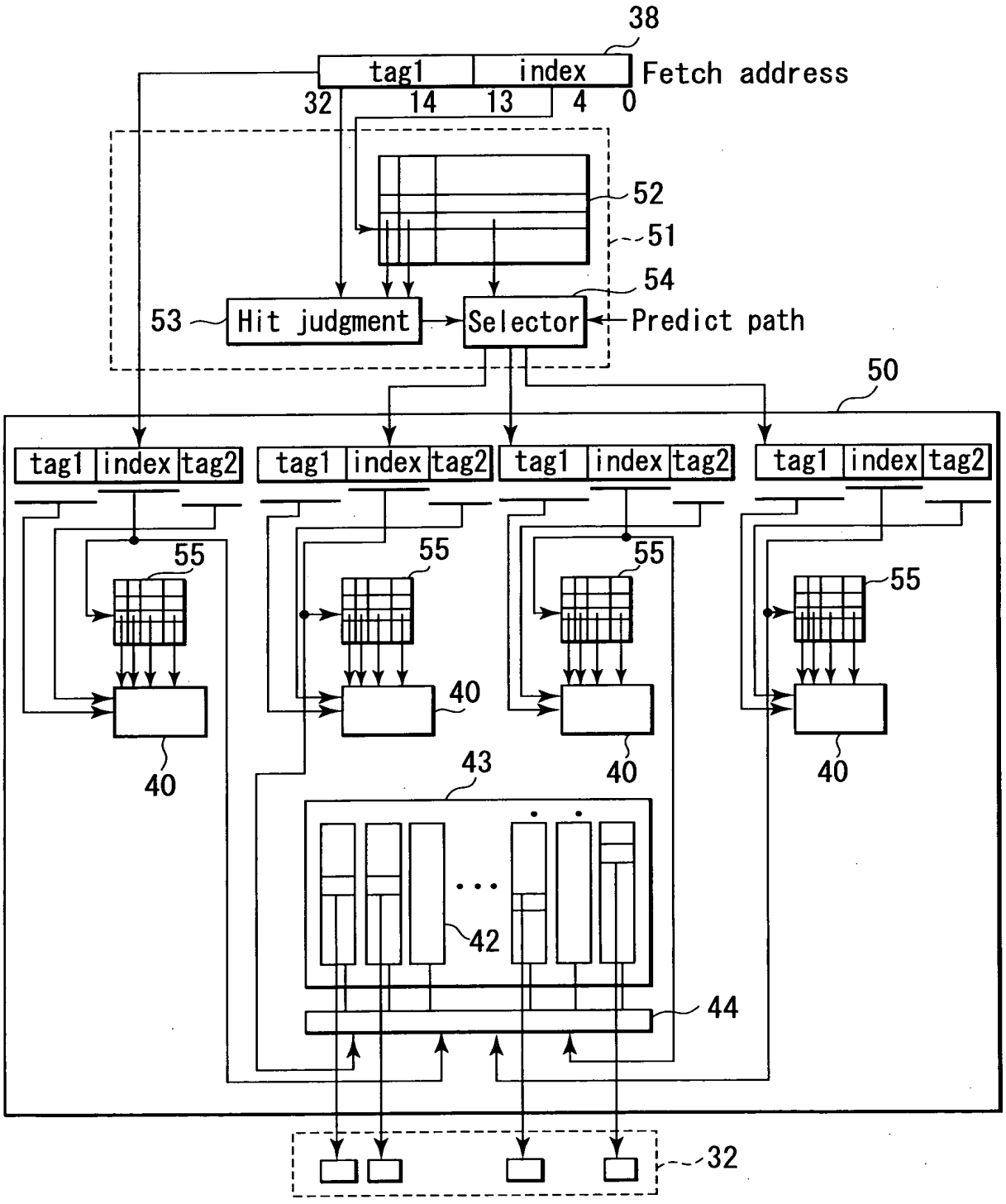
38
tag1
index
Fetch address
32
14
13
4
0
52
51
54
53
Hit judgment
Selector
Predict path
50
tag1
index
tag2
55
40
43
42
44
32

FIG. 25

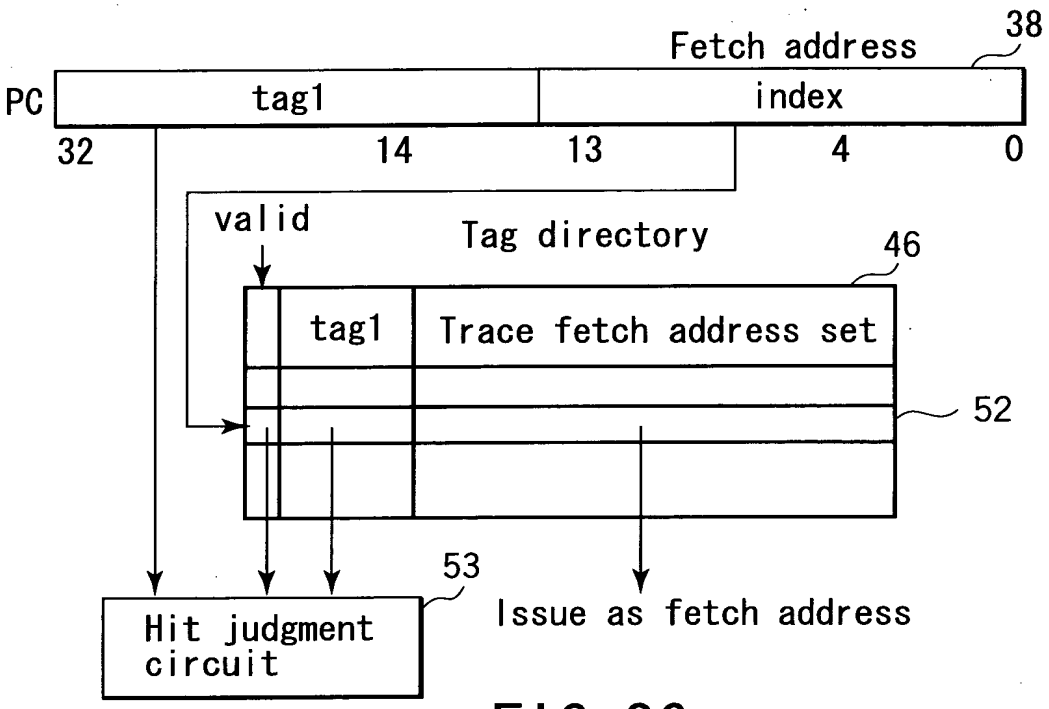
Fetch address
38
PC
tag1
index
32
14
13
4
0
valid
Tag directory
46
tag1
Trace fetch address set
52
53
Hit judgment circuit
Issue as fetch address

FIG. 26

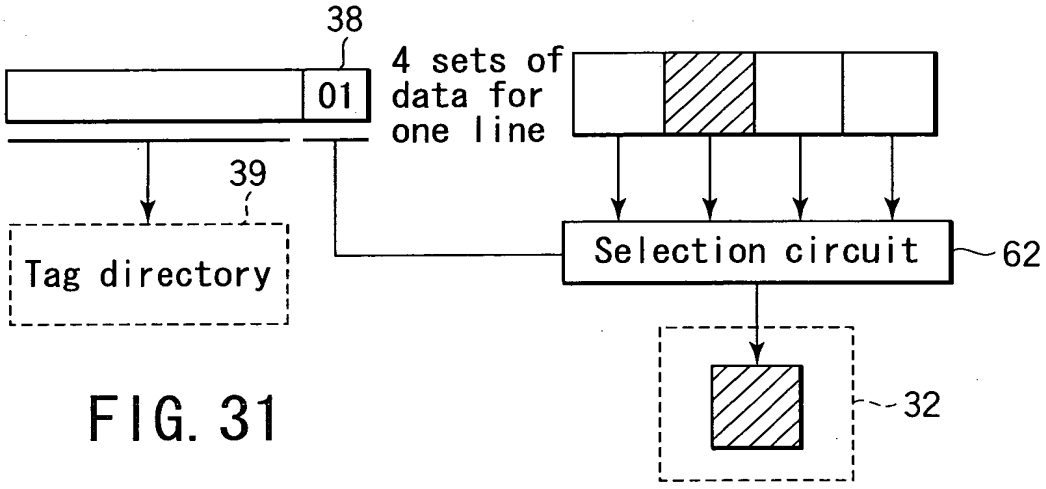
38
01
4 sets of data for one line
39
Tag directory
Selection circuit
62
32

FIG. 31

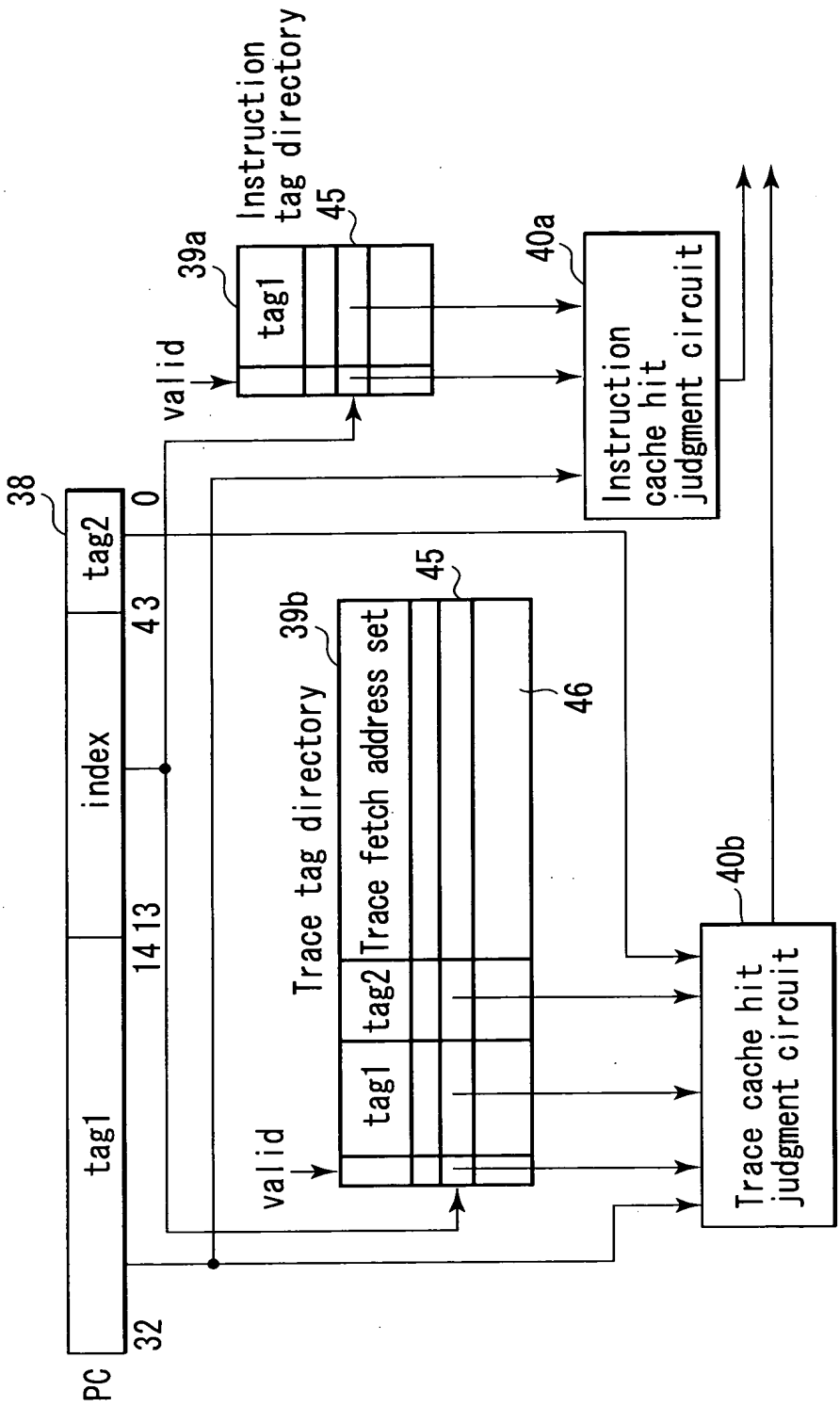
PC
32
38
tag1
index
tag2
14 13
4 3
0
valid
39a
tag1
Instruction tag directory
45
40a
Instruction cache hit judgment circuit
valid
39b
tag1
tag2
Trace fetch address set
Trace tag directory
45
46
40b
Trace cache hit judgment circuit

FIG. 27

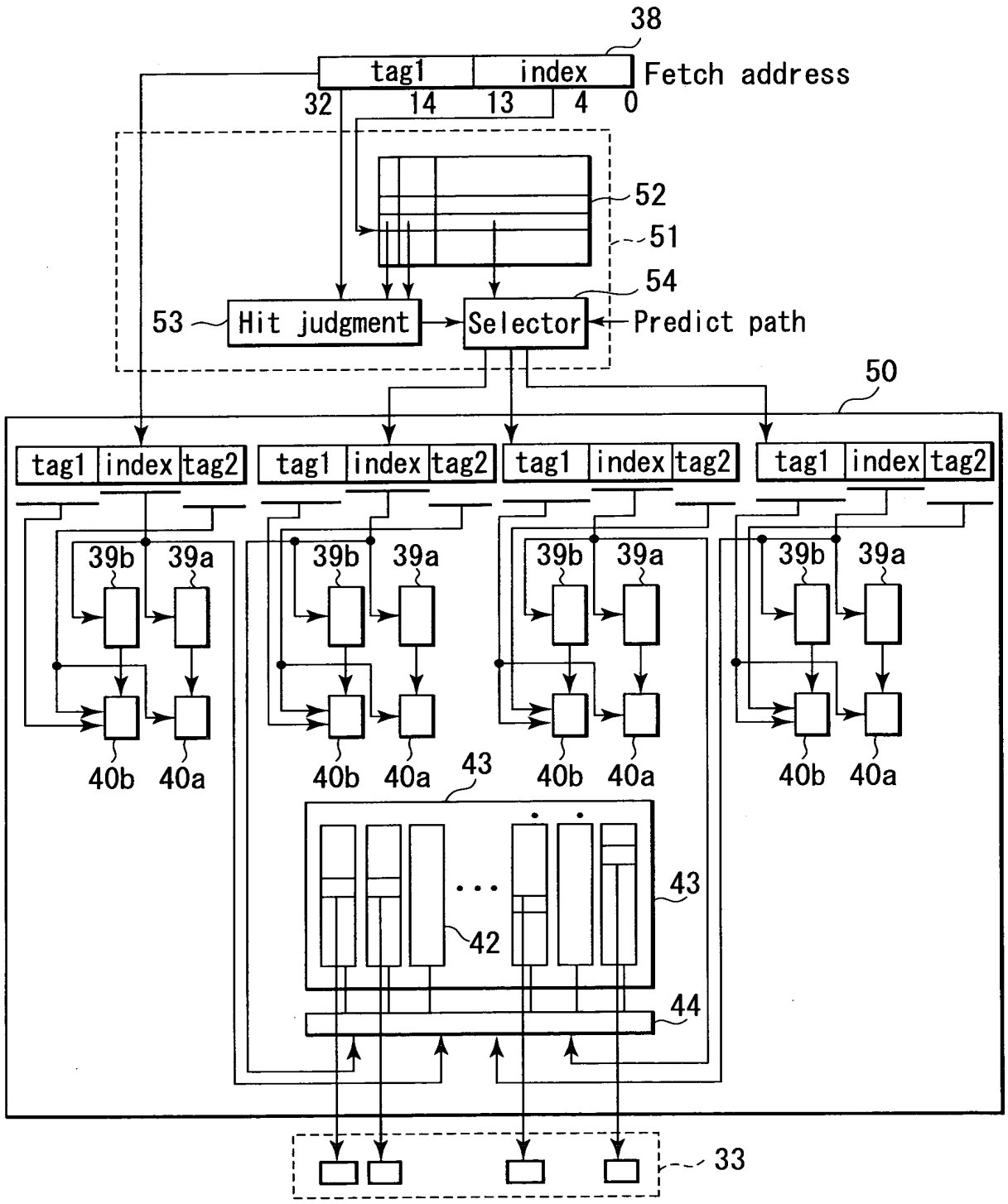
38
tag1
index
Fetch address
32
14
13
4
0
52
51
54
53
Hit judgment
Selector
Predict path
50
tag1
index
tag2
39b
39a
40b
40a
43
42
44
33

FIG. 28

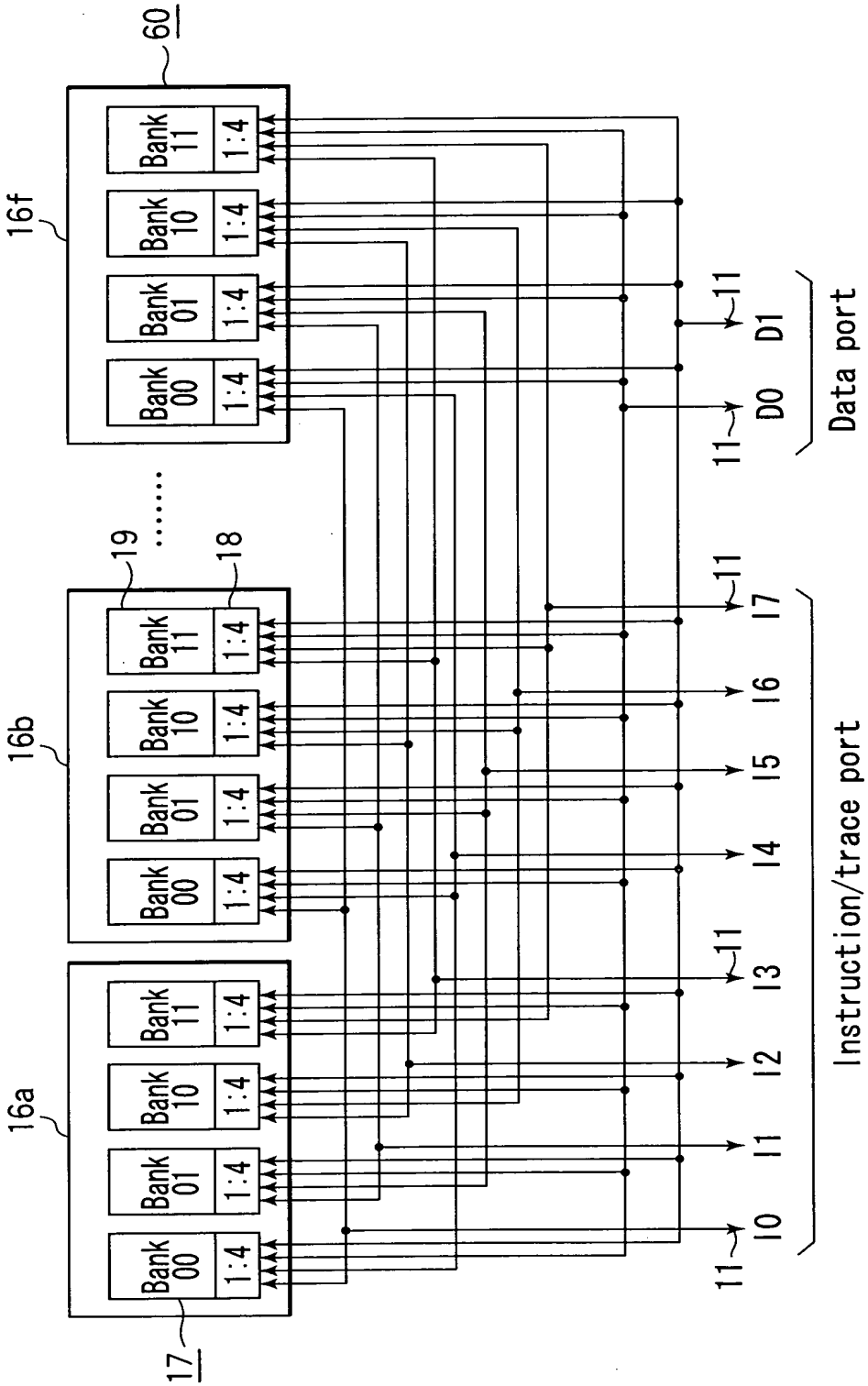
60
16f
16b
16a
17
19
18
Bank 11
Bank 10
Bank 01
Bank 00
1:4
11
D1
D0
Data port
I7
I6
I5
I4
I3
I2
I1
I0
Instruction/trace port

FIG. 29

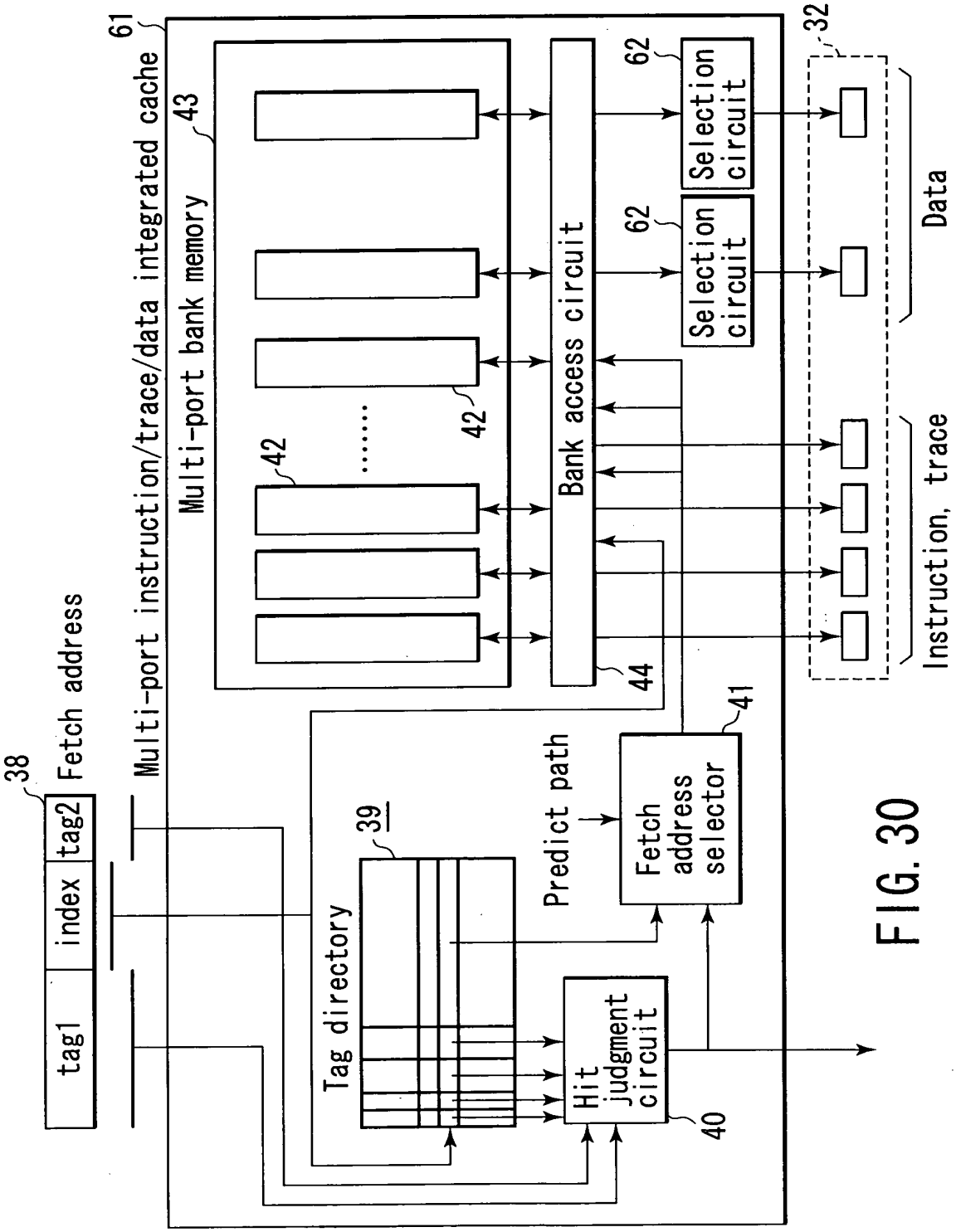
61
Multi-port instruction/trace/data integrated cache
43
Multi-port bank memory
42
42
Bank access circuit
44
62
Selection circuit
62
Selection circuit
32
Data
Instruction, trace
38
Fetch address
tag1
index
tag2
39
Tag directory
Predict path
41
Fetch address selector
Hit judgment circuit
40

FIG. 30